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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,317	10/28/2003	Douglas C. Buhler	10020953-1	4870

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,317	BUHLER ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 and 11-32 is/are rejected.

7)☒ Claim(s) 10 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 28 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: _____.

DETAILED ACTION

1. Claims 1-32 are pending in the application.

Specification

2. Claim 4 is objected to because of the following informalities:

Said claim recites "the second plurality of delay units" which appears to be lacking antecedent basis. However, said limitation appears to be referring to the same in claim 11; therefore, claim 4 will be understood to depend on claim 11.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5, 8, 9, 12-20, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens (U.S. Pat. No. 5,465,065).

Stevens, for example in Fig. 4, discloses a circuit and a related method for determining the propagation delay of an integrated circuit, comprising: a first rank of logic memory elements (D flip-flops 94A-94E), each logic memory element having a data input (D input), a data output (inherent in D flip-flops), and a clock input (C input), the clock inputs being coupled together and configured to be driven by a clock signal (applied at 68 and 96); a plurality of delay units

(82, 84, 86, 88 and 90) coupled in series, each delay unit having an input and an output, the output of each delay unit configured to drive the data input of one of the logic memory elements (for example, the output of 82 driving 94A); wherein each of the plurality of delay units exhibit the same amount of delay (or in a linear fashion, as implied in column 4, lines 15-25); further comprising a preliminary delay unit (for example, 70, 72, 74, 76, 78 and 80).

However, Stevens does not disclose a logic inverter having an input configured to be driven by the clock signal, the inverter having an output configured to drive the input of the first delay unit of the plurality of delay units; that the preliminary delay unit is positioned either before or after the inverter; and that each delay unit comprises a plurality of logic inverters coupled in series.

Since Stevens discloses negative-edge-triggered flip-flops (94A-94E in Fig. 4), and since positive-edge-triggered flip-flops were common and well-known in the art as an equivalent means for capturing and storing data, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the circuit of Stevens by substituting the negative-edge-triggered flip-flops with positive-edge-triggered flip-flops as an equivalent alternative and including a logic inverter either before or after the preliminary delay unit to essentially obtain the same function and result. Such modification to a logic circuit using an inverted logic configuration to essentially obtain a same effect and result was common and common and well known in the art and would have been within the ordinary skill in the art. Further, use of logic inverters in series for a delay unit was common and well known in the art.

5. Claims 6, 7, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens (U.S. Pat. No. 5,465,065) in view of Horowitz et al. ("The Art of Electronics", Cambridge University Press, 1980, pages 343-344).

Stevens discloses a circuit as recited in claims 1 and 19, with the exception of a second rank of logic memory elements, each logic memory element of the second rank having a data input, a data output, and a clock input, the clock inputs being coupled together and configured to be driven by the clock signal, the data input of each logic memory element of the second rank configured to be driven by the data output of one of the logic memory elements of the first rank, wherein each logic memory element of the second rank comprises a D flip-flop.

Horowitz, for example in Fig. 8.45A on page 344, discloses a second D flip-flop logic memory element (the slave flip-flop on the right side of the dashed line) having a data input (an input M at 5), a data output (Q), and a clock input (connected to 5 and 6) driven by a clock signal (CLK), the data input of the second logic memory element configured to be driven by the data output (the output M from 3) of a first D flip-flop logic memory element (the master flip-flop on the left side of the dashed line).

Since the master-slave flip-flop configuration was common and well known in the art (see for example Horowitz, page 343, column 2, the middle paragraph), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to couple a second rank of D flip-flops in the circuit of Stevens, one for each of the first rank of D flip-flops, in a master-slave configuration as in Horowitz, for the purpose of reliably and stably capturing and storing the propagation data.

6. Claims 4, 11, 24-28 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens (U.S. Pat. No. 5,465,065) in view of Miura (U.S. Pat. No. 6,756,833).

Stevens discloses a circuit and a related method as recited in claims 1, 12 and 29, with the exception of a multiplexer having data inputs, selector inputs, and a data output; a second plurality of delay units coupled in series, each delay unit of the second plurality of delay units having an input and an output, the output of each delay unit of the second plurality of delay units configured to drive one of the inputs of the multiplexer; and a microprocessor configured to read the data output of each of the logical memory elements and to select one of the data inputs of the multiplexer via the selector inputs for gating to the output of the multiplexer (i.e., a means for tuning the speed of a critical signal based on the stored logical state for each of the delayed inverted clock signals); wherein each delay unit of the second plurality of delay units comprises a plurality of logic inverters coupled in series.

Miura, for example in Fig. 3, discloses a multiplexer (15), a second plurality of delay units in series (12), each comprising a plurality of logic inverters in series (see column 3, lines 53-57), and a microprocessor (21), for tuning the speed of a critical signal (INPUT SIGNAL A).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate the circuit of Stevens in a system such as that of Miura, such that the propagation delay information stored in the logic memory elements of Stevens would be accessed by the CPU to select one of the delayed signals (as in Miura), for the purpose of efficiently and accurately adjusting the signal delays under various ambient conditions, such as changes in the operating temperature, the power supply voltage, etc. (see for example Stevens, column 2, lines 22-34, and Miura, column 1, lines 35-42).

7. Claims 23 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens (U.S. Pat. No. 5,465,065) in view of Baumann (U.S. Pat. No. 5,744,992).

Stevens discloses a circuit and a related method as recited in claims 12 and 29, with the exception of a means for forcing the stored logical state of each of the delayed inverted clock signals to collectively display a single logical transition indicating the propagation delay of the integrated circuit.

Baumann, for example in Fig. 1, discloses a means for forcing a stored logical state (in flip-flops 131-146) of each of the delayed clock signals (at the outputs of 111-126) to collectively display (as outputs 171-185) a single logical transition indicating the propagation delay (i.e., detecting only the leading edge of the propagated signal, via 151-165; see also column 4, lines 4-17).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate Baumann's means for displaying a single logical transition indicating the propagation delay, for the purpose of accurately determining the propagation delay in a slow signal path (wherein multiple transition edges may occur).

Allowable Subject Matter

8. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 10, the prior arts of record do not disclose or suggest a circuit as recited in claim 10, and particularly, a plurality of AND gates, each AND gate being associated with one of the series of delay units, each AND gate having an output configured to drive the data input of the logic memory element of the first rank associated with the delay unit associated with the AND gate, each AND gate having a first input configured to be driven by the output of its associated delay unit and a second input configured to be driven by the output of the logic memory element of the first rank associated with the delay unit immediately preceding the delay unit associated with the AND gate, the second input of the AND gate associated with the first delay unit of the series of delay units being configured to be driven by a logic HIGH.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kocis et al. (U.S. Patent No. 5,245,231) discloses a delay calibration circuit.

Takaki et al. (U.S. Patent No. 5,534,808) discloses a signal delay circuit.

Yazawa et al. (U.S. Patent No. 6,720,811) discloses a delay correction circuit.

Parry et al. (U.S. Patent No. 6,680,636) discloses a delay measurement circuit.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

VAN THU NGUYEN
PRIMARY EXAMINER